ISS Gary Patton Keynote: FD-SOI, FinFETS, and Beyond!

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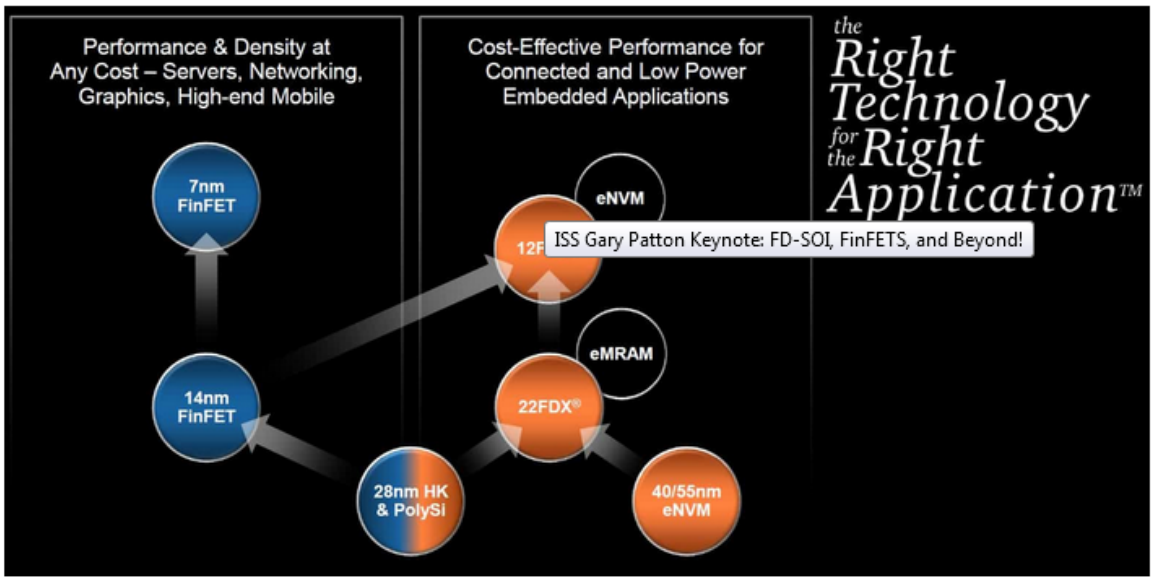
Two weeks ago the SEMI ISS Conference was held at Half Moon Bay in California. On the opening day of the conference Gary Patton CTO of GLOBALFOUNDRIES gave the keynote address and I also had the chance to sit down with Gary for an interview the next day.



Gary started his keynote by discussing the big merger and acquisition trend in the industry. Money can go into R&D, facilities, stock buy backs or M&A. Facilities and R&D are long return investments, M&A shows a quicker return.

Worldwide traditional PC shipments are shrinking and Smartphone growth is slowing. Where will growth come from?

- Internet of Things - servers will be needed to handle all the data.
- Automotive - driver assist and self-driving cars.
- 5G - will offer 10Gb/sec with 1ms latency.
- Augmented Reality/Virtual Reality - moving from high end gaming to the mainstream.
- Artificial Intelligence (AI) - the preceding items all create data, AI can produce useful results from the data.

Clients, networks and data centers will need a range of technologies, GLOBALFOUNDRIES offers choices.

- Advanced packaging, ASICs, RF, silicon photonics, and a leading-edge development team all came over in the IBM acquisition.
- GLOBALFOUNDRIES offers FinFETs and FDSOI - you need both to optimize for different applications. FinFETs offer a lot of drive current and lots of performance but you must be able to amortize $250 million dollars in design costs. FDSOI is optimized for low power and low design cost.

With FDSOI, forget everything you knew with PDSOI, FDSOI offers 40% less masks than a comparable FinFET. For smaller chips FDSOI offers low voltage and leakage and is very flexible. With a thin silicon layer and thin buried oxide you can body bias the device under software control. Analog design is easier than for FinFETs where you must work in increments of fins. FDSOI also offer Ft/Fmax of around 350Ghz versus 150-200 Ghz for FinFETs providing superior RF performance. You can design with a small watchdog processor that is always on and use reverse body bias for the rest of the circuit to minimize leakage current while it is off.

GLOBALFOUNDRIES is ramping up their 22FDX platform, it is ideal for IoT, mobile and RF applications with FinFET like performance at 28nm cost. 22FDX has 0.4 volt operation for low power, 1pA/micron ultra-low leakage, software body bias control and excellent RF performance. 22FDX can achieve 70% lower power than 28nm, and a 20% smaller die, there are also 40% fewer masks than 16/14nm FinFETs at a 20% lower cost.

Beyond 22FDX GOBALFOUNDRIES offers 12FDX, the industry's first FDSOI roadmap with full node scaling. Once it is available 12FDX will offer a new standard for RF and analog integration and will enable intelligent clients, 5G, AR/VR, Automotive and AI solutions. The decisions to do 22nm versus 20nm and 12nm versus 10nm for FDSOI keep mask counts down at the cost of a "little bit of density".

GLOBALFOUNDRIES has a big focus on building accelerator IP for body biasing to enable design for both 22FDX and 12FDX. The transition from 28nm to 22FDX and 12FDX design is easier than the transition to FinFETs because it is planar to planar.

GLOBALFOUNDRIES 7nm process is currently in development and is targeted at server/data centers, networking such as 5G infrastructure, and high end mobile application processors. From 14nm to 7nm device performance will be increased by >30%, total power reduced by >68%, density by >2x and it will provide a 30% die cost reduction. Later on Monday multiple presenters talked about Moore's law being dead and yet here is GLOBALFOUNDRIES continuing to improve density, performance and cost. During our interview, Tuesday morning I told Gary I didn't believe Moore's law was dead and he agreed with me. The 7nm process has an optimized Fin profile, super steep wells, multiple work functions, source drain epi optimization, low-k spacers, and cobalt middle of line.

During our interview, I discussed the multiple work function approach with Gary and he confirmed that the threshold voltages are all set by work functions without using threshold adjust implants. Initial FinFET processes have all used threshold adjust implants to set multiple threshold voltages. The drawback to implants is that they are subject to random dopant fluctuations making precise threshold voltage control difficult. Also, implanting into the channel reduces mobility. Introducing work function control of threshold voltages is an integration challenge but should provide better performance. I noted that with processes commonly requiring many threshold voltages this must be a lot of different metals and Gary said it was metals or combinations of metals.

Two other areas I asked Gary about were the use of a strain relaxed buffer (SRB) and SAQP patterning. At IEDM there was an Alliance paper on 7nm (IBM, GLOBALFOUNDRIES and Samsung) and I asked Gary if GLOBALFOUNDRIES was going to the use the SRB discussed in that paper and he said they weren't discussing that yet. I also asked about the lithography approach for this process. Gary has previously discussed that this is an optical lithography based process with up to SAQP. I asked him if he could discuss whether they used SAQP in the backend. I have previously speculated that GLOBALFOUNDRIES might want to limit the minimum metal pitch to 40nm to avoid having to use SAQP on multiple metal layers. Gary said he couldn't discuss that.

In his keynote Gary did discuss the difficulty of scaling optical lithography to 7nm, 14nm was around 60 masks, 10nm around 70 masks and 7nm around 80 masks! The 7nm process is designed to be EUV compatible when it is ready and EUV can reduce 30 critical masks to 10 masks providing a 30 day improvement in cycle time (around 1.5 days per mask). EUV still needs more sensitive photoresists that also provide good LER, and masks must be defect free. The analogy Gary offered is the equivalent of a golf ball sized defect in an area equivalent to California would be a disaster. They need to be able to inspect masks and they need pellicles to prevent added particles on the masks. The promise of EUV is to eliminate triple/quadruple patterning that is very painful for designers.

Beyond FinFETs around 2020 Gary discussed a transition to gate all around (GAA) will be required in the form of horizontal or vertical nanowires. Horizontal nanowires are constrained by horizontal dimensional scaling, vertical is more challenging from an integration perspective but has easier channel scaling.

Beyond these processes there is work on system level integration using advanced packaging to integrate passives, ICs and silicon photonics. As bandwidth and distance go up photonics becomes more critical. Burlington and Singapore make photonics and East Fishkill is working on it.

GLOBALFOUNDRIES is also doing a lot of work with AMD on design-technology co-optimization.

In summary Gary presented a view of a future for the semiconductor industry with new applications driving growth and a continuation of Moore's law in the form of process performance, density and cost improvements. GLOBALFOUNDRIES is positioning themselves as a unique supplier that offers roadmaps for continued improvement in both FinFET and FDSOI technologies.